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FIG. 1
SoC ASIC

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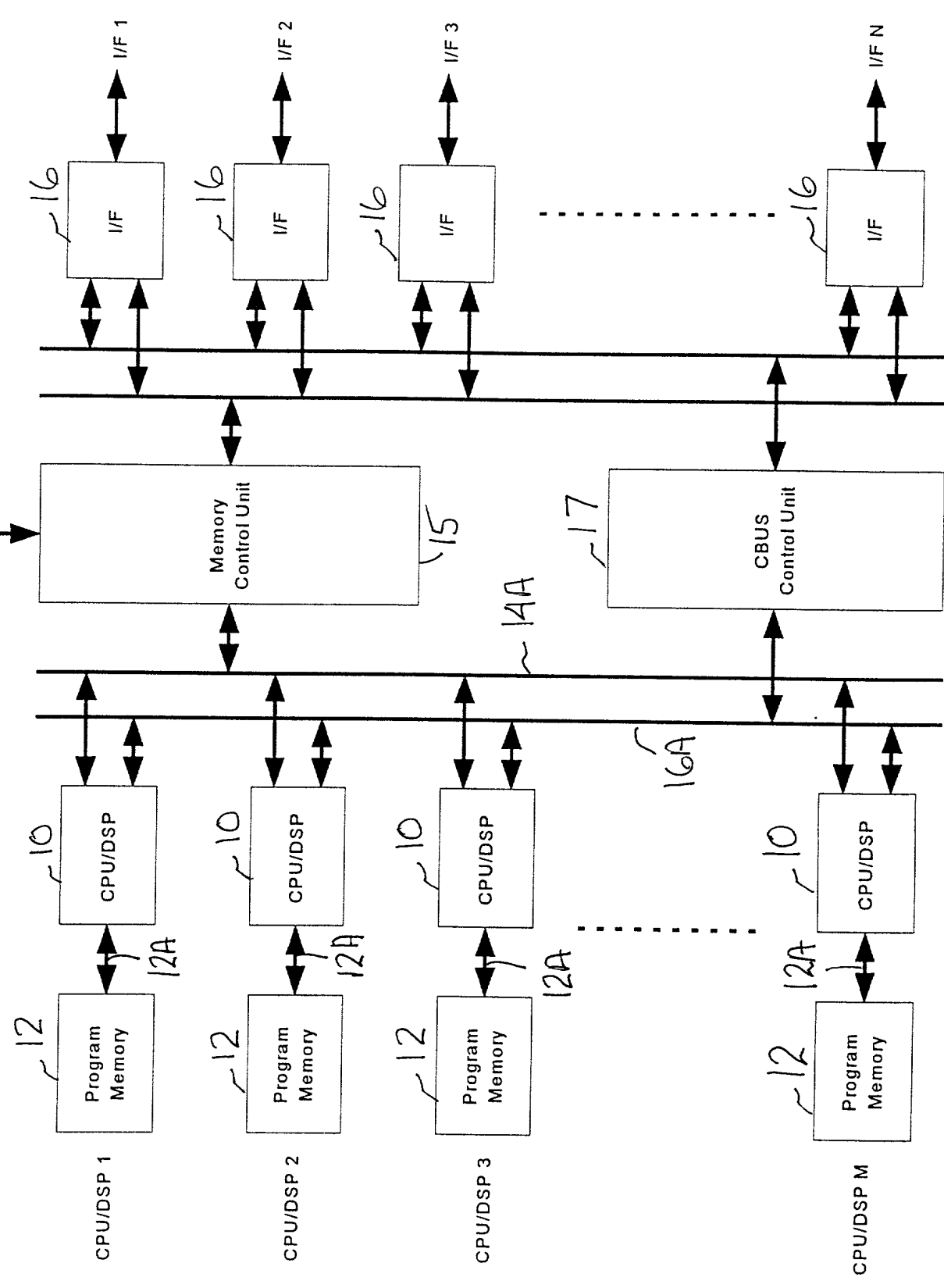


FIG. 1

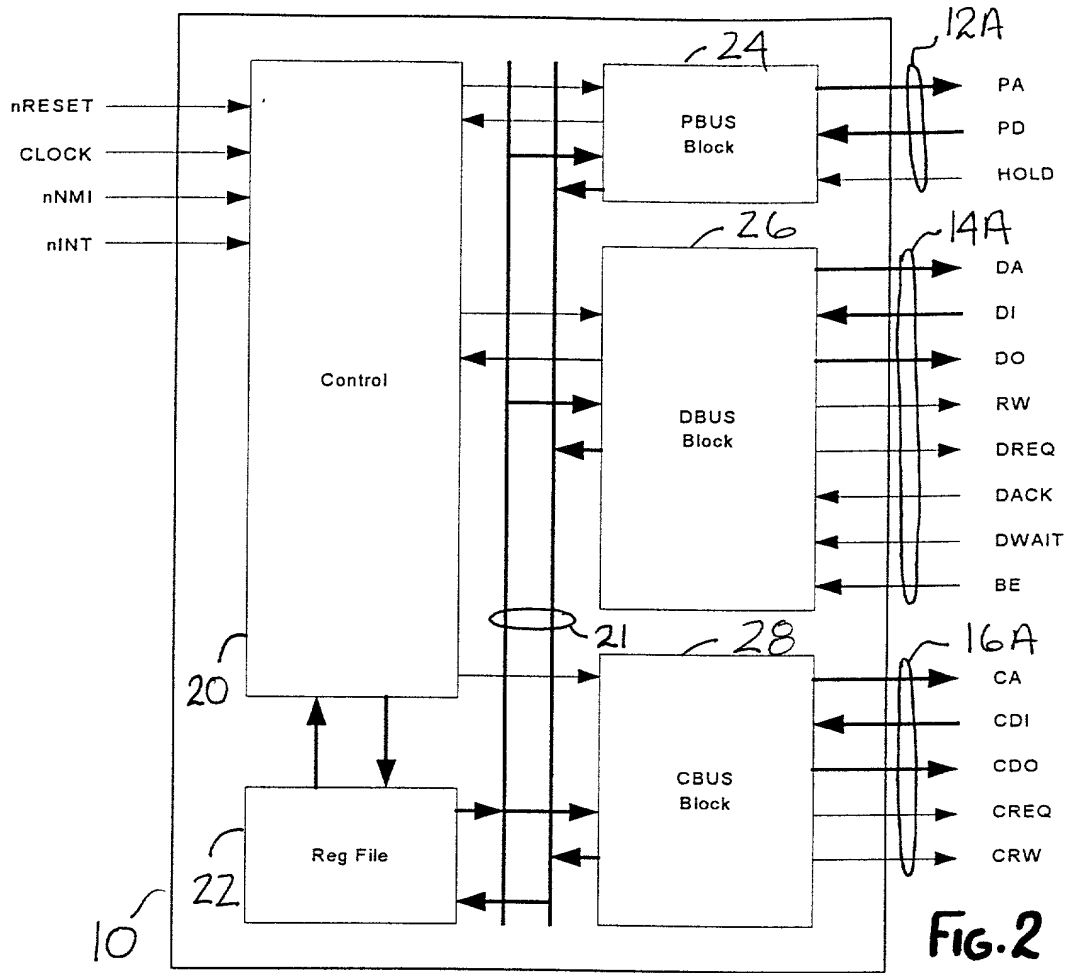


FIG. 2

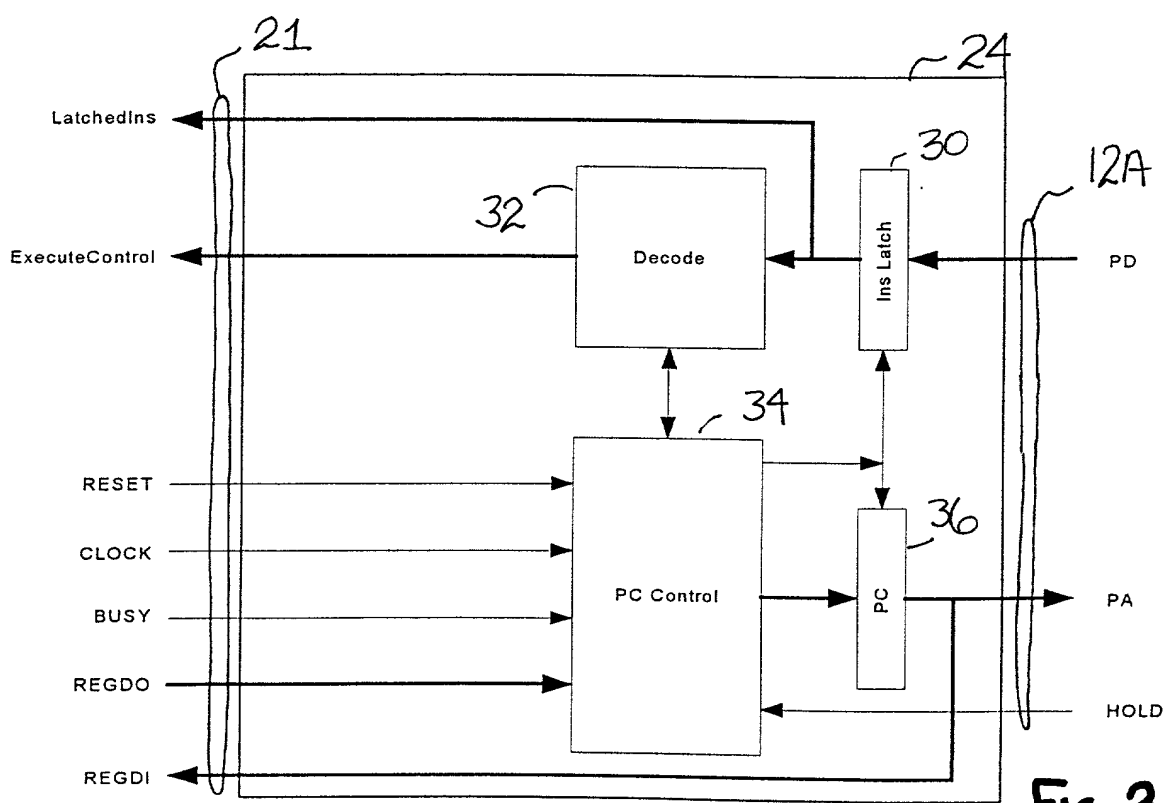


FIG. 3

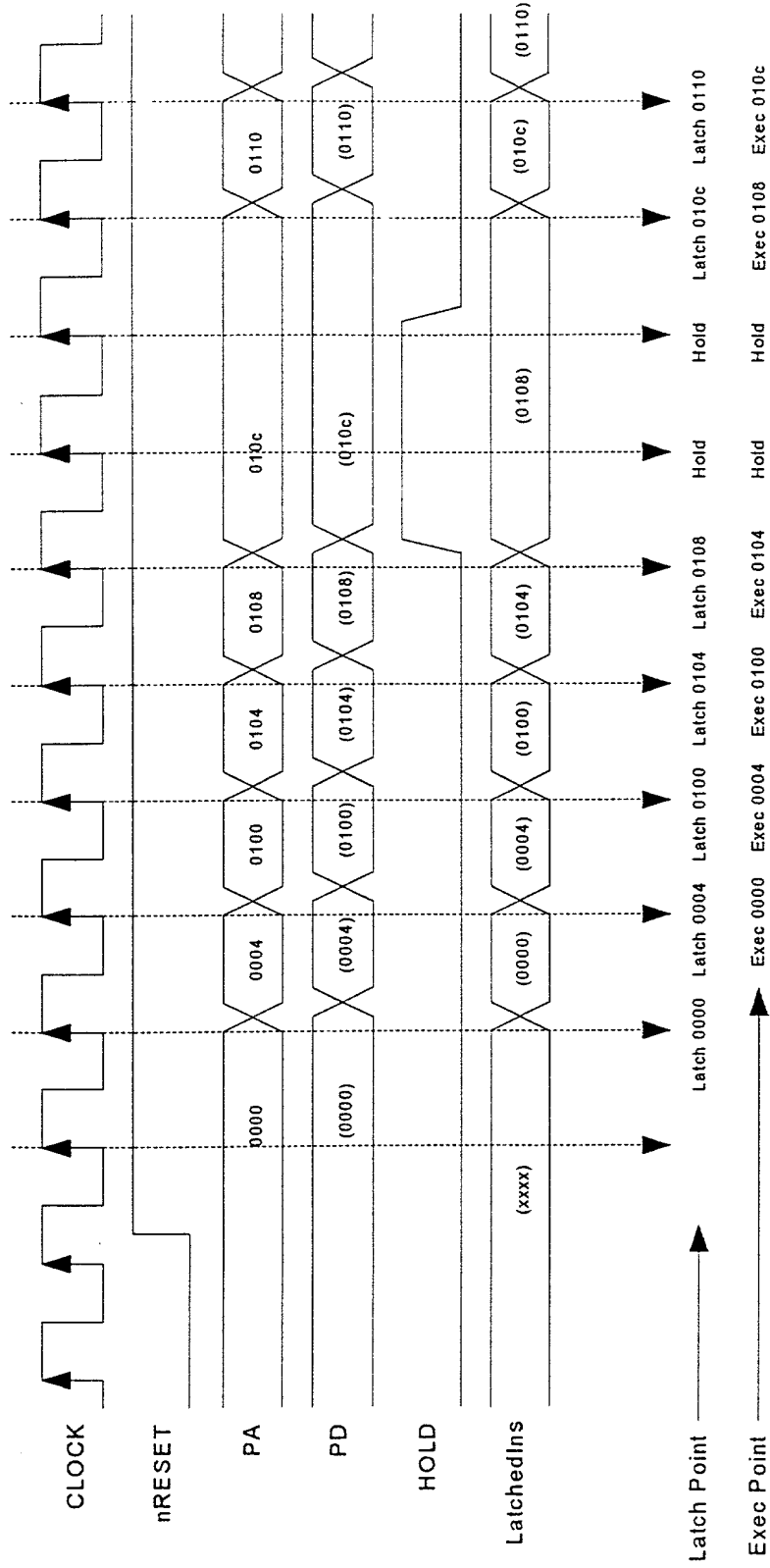
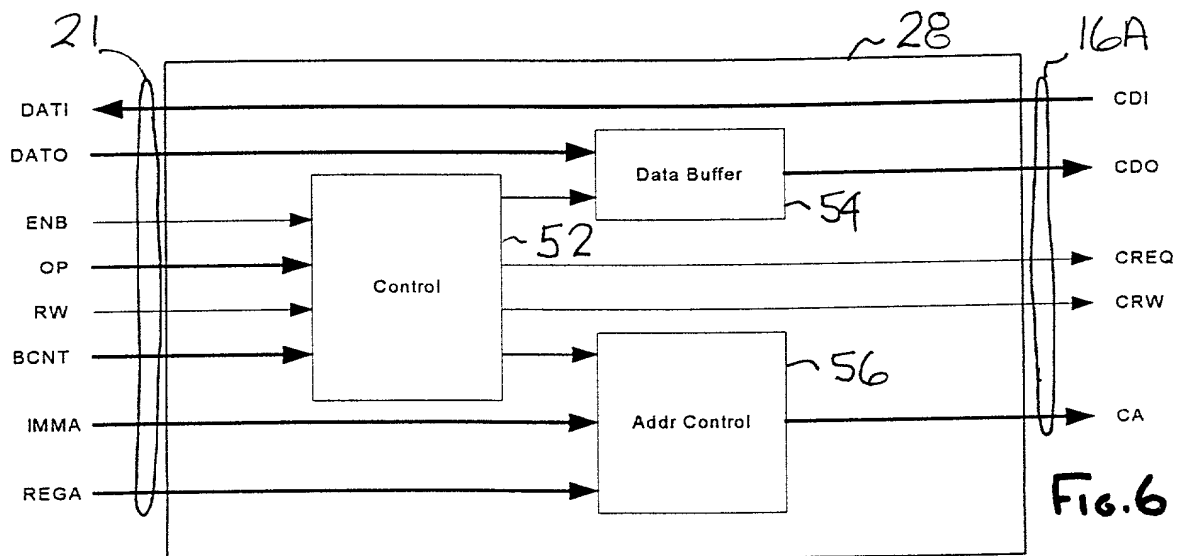


FIG. 4

The diagram illustrates a microprocessor system with the following components and connections:

- Internal Components:**
 - Control (42):** Receives external control signals (ENB, OP, STB, BCNT) and sends signals to the Data Control, Data Buffer, and Address Selection logic.
 - Data Control (40):** Manages data flow between the Data Buffer and the external data bus.
 - Data Buffer (44):** Buffers data between the internal system and the external data bus.
 - Destination Addr Control (46):** Receives the DADR signal and outputs the Destination Address to the Address Selection logic.
 - Source Addr Control (48):** Receives the SADR signal and outputs the Source Address to the Address Selection logic.
 - Address Selection (50):** Receives the Destination and Source addresses and outputs the final DA signal.
- External Signals:**
 - Input Signals (21):** REGDI, REGDO, ENB, OP, STB, BCNT, DADR, DREGC, SADR, SREGC.
 - Output Signals (14A):** DI, DO, DREQ, SIZE, DACK, BE, WAIT, DRW, DA.



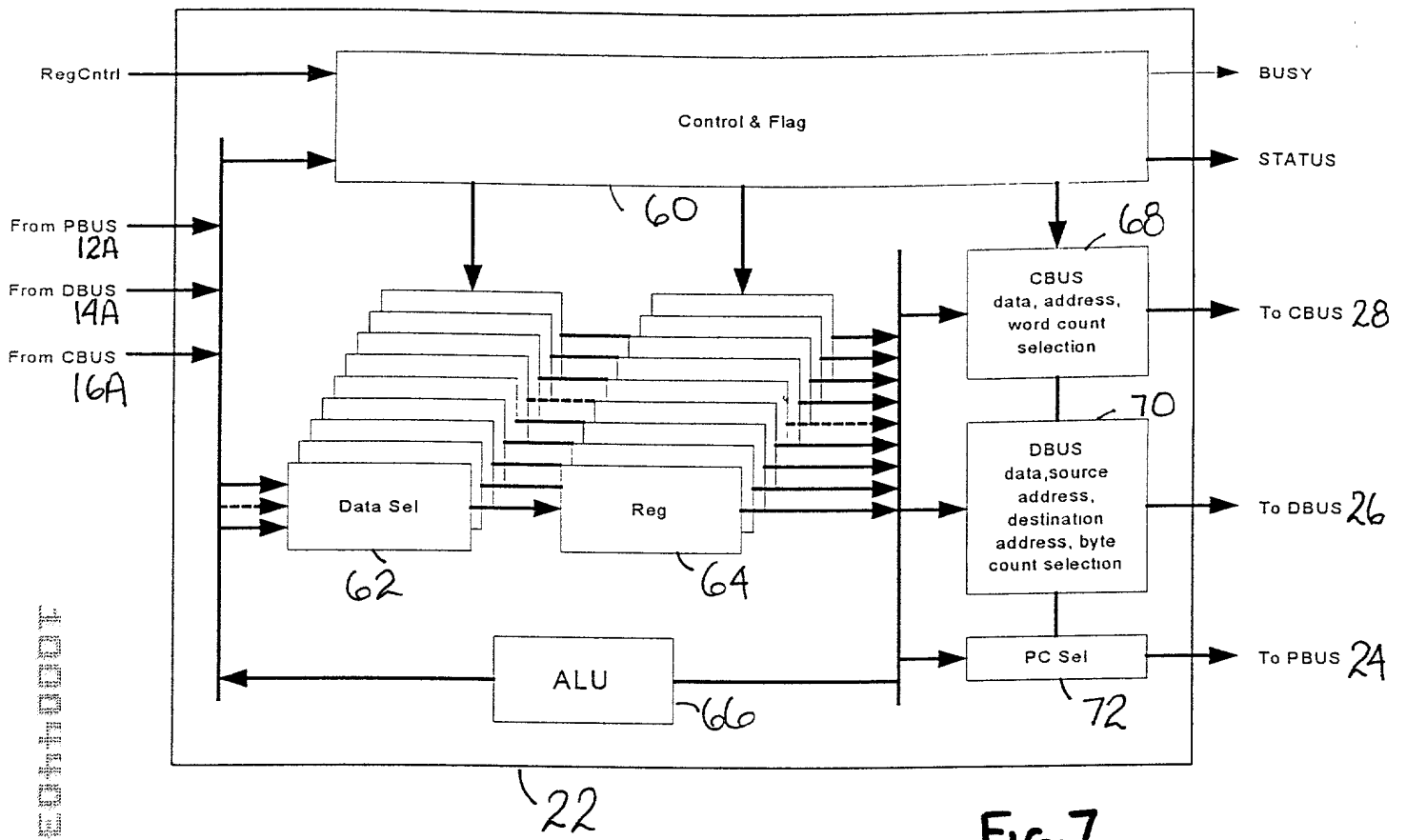


FIG. 7

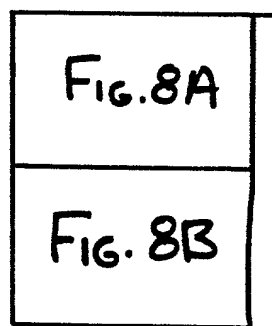


FIG. 8

FIG. 8A

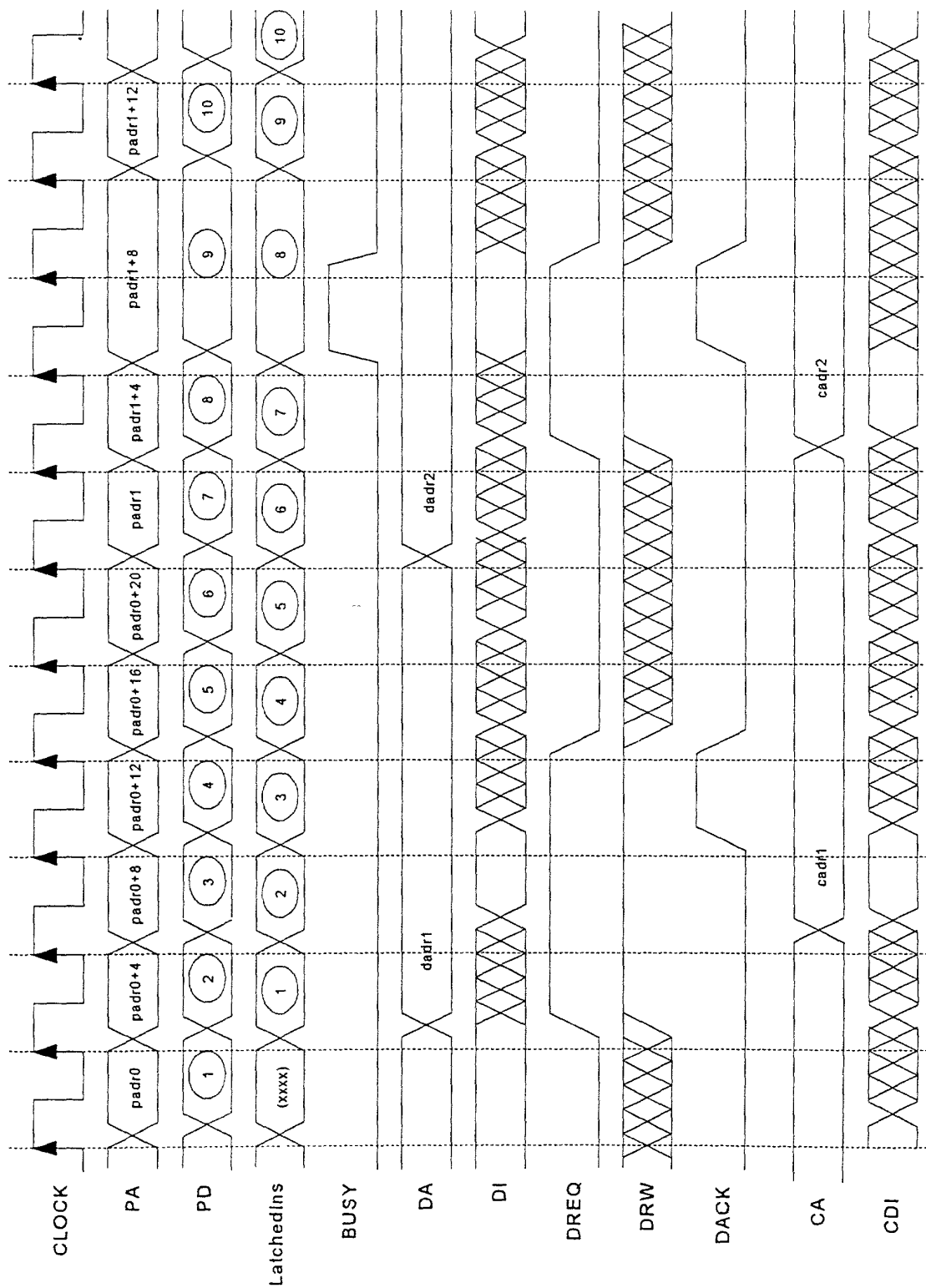


FIG. 8B

FOR COUNTER

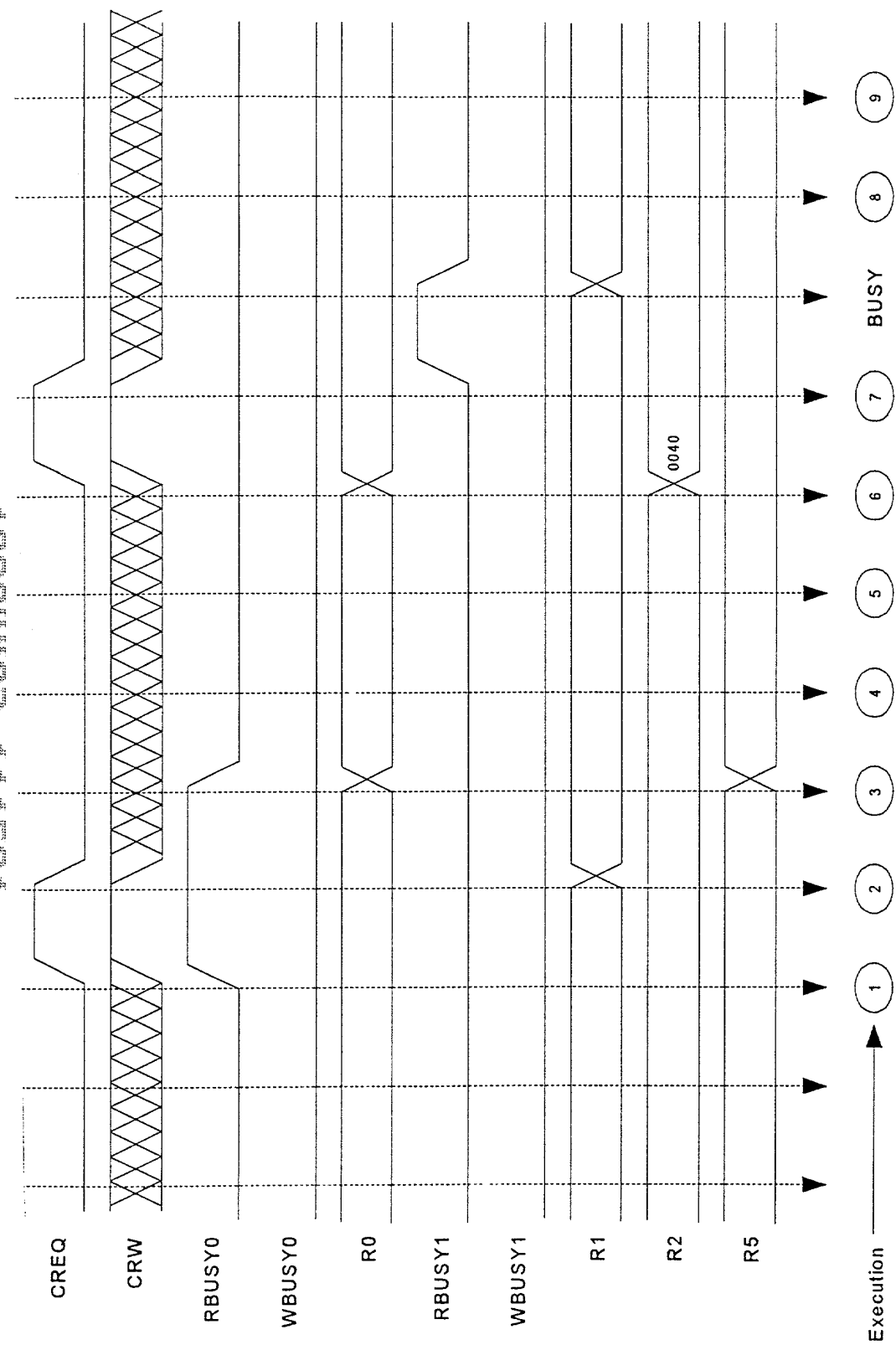


FIG. 9

5 WIRELESS COMMUNICATIONS SYSTEM

